Docket No.: 1309.43598X00

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Application of:

Hiroshi SUZUKI et al.

Serial No. 10/790,140

Filed: March 2, 2004

For: DISK ARRAY DEVICE AND METHOD OF CHANGING THE CONFIGURATION OF THE DISK

PETITION TO MAKE SPECIAL
UNDER 37 CFR §1.102(MPEP §708.02)

April 22, 2005

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants hereby petition the Commissioner to make the above-identified application special in accordance with 37 CFR §1.102(d). Pursuant to MPEP §708.02(VIII), Applicants state the following.

(A) This Petition is accompanied by the fee set forth in 37 CFR §1.17(h). The Commissioner is hereby authorized to charge any additional payment due, or to credit any overpayment, to Deposit Account No. 50-1417.

(B) All claims are directed to a single invention. If the Office determines that all claims are not directed to a single invention, Applicant will make an election without traverse as a prerequisite to the grant of special status.

(C) A pre-examination search has been conducted.

The search was directed to the invention set forth in claims 1-8. As set forth in claim 1, the invention is related to a disk array device comprising: a channel adapter that controls data transmission and reception with a high-order device; a storage device that stores data; a storage device control board to which the storage device is connected; a disk adapter that is connected to the storage device via the storage device control board and controls data transmission and reception with the storage device; and a management unit that is respectively connected to the disk adapter and the channel adapter, wherein the storage device control board includes a connection circuit that is connected to the storage device, and switch circuits that are respectively disposed at an input side and an output side of the connection circuit and are switchable between a connected mode where they are connected to another adjacent storage device control board and an independent mode where they are separated from the other adjacent storage device control board, and the switch circuits are switchable between the connected mode and the independent mode by an output signal from the management unit.

The search of the above features was conducted in the following areas: class 710, subclasses 62 and 315-317, class 711, subclass 111-114, 120, 147, 148, 151-154, 170 and 203 and class 714, subclasses 5-7.

Additionally, a computer database search was conducted on the USPTO system EAST.

(D) The following is a list of the references deemed most closely related to the subject matter encompassed by the claims:

U.S. Patent Number	Inventors
5,960,455	Bauman
6,006,296	Gold et al.
6,425,049	Yamamoto et al.
6,813,676	Henry et al.

U.S. Patent Publication No.	Inventor(s)
2001/0054133	Murotani et al.
2002/0023195	Okada
2004/0024951	Aruga
2004/0034737	Fujimoto et al.
2004/0083338	Moriwaki et al.
2004/0111560	Takase et al.

A copy of each of these references (as well as other references uncovered during the search) is enclosed in an accompanying IDS.

(E) It is submitted that the present invention is patentable over the references for the following reasons.

It is submitted that the cited references, whether considered alone or in combination, fail to disclose or suggest the invention as claimed. In particular,

the cited references, at a minimum, fail to disclose or suggest a storage device control board to which the storage device is connected, and/or switch circuits that are respectively disposed at an input side and an output side of the connection circuit and are switchable between a connected mode where they are connected to another adjacent storage device control board and an independent mode where they are separated from the other adjacent storage device control board, and/or the switch circuits are switchable between the connected mode and the independent mode by an output signal from the management unit, and/or in a case where a connected mode instruction/signal is issued from the management unit, the storage devices are together connected to each other and to the same disk adapter, and/or in a case where an independent mode instruction/signal is issued from the management unit, the storage devices are divided into plural storage device groups and the storage device groups are respectively connected to different disk adapters.

All of the independent claims recite at least one of these features or this feature, if there is only one. In particular, independent claim 1 recites a storage device control board to which the storage device is connected, switch circuits that are respectively disposed at an input side and an output side of the connection circuit and are switchable between a connected mode where they are connected to another adjacent storage device control board and an independent mode where they are separated from the other adjacent storage device control board, and the switch circuits are switchable between the connected mode and the independent mode by an output signal from the management unit. Independent

claim 7 recites in a case where a connected mode instruction is issued from the management unit, the storage devices are together connected to each other and to the same disk adapter, and in a case where an independent mode instruction is issued from the management unit, the storage devices are divided into plural storage device groups and the storage device groups are respectively connected to different disk adapters. Independent claim 8 recites plural storage device control boards that are respectively disposed on the attachment-use board and connected to the storage device, a first switch circuit that is disposed at an input side of the connection circuit, a second switch circuit that is disposed at an output side of the connection circuit, and in a case where a connected mode signal is inputted from the outside, the storage device control boards become usable with being connected to each other via the switch circuits, and in a case where an independent mode signal is inputted from the outside, the storage device control boards become usable with being respectively separated.

The references considered most closely related to the claimed invention are briefly discussed below:

U.S. Patent No. 5,960,455 (Bauman) discloses a general purpose digital data processing system that employs one or more storage controllers shared among multiple instruction processors and input/output processors in a multi-processor system. The computer system uses a storage controller having a high performance interconnect scheme that scales in system performance as additional common storage controller modules are added. (See, e.g., Abstract

and column 2, lines 33-59.) However, unlike the present invention, Bauman does not disclose a disk array device that includes storage device control boards having a connection circuit that is connected to a storage device, and switch circuits that are respectively disposed at an input side and an output side of the connection circuit and are switchable between a connected mode where they are connected to another adjacent storage device control board and an independent mode where they are separated from the other adjacent storage device control board, wherein the switch circuits are switchable between the connected mode and the independent mode by an output signal from a management unit.

U.S. Patent No. 6,006,296 (Gold et al.) discloses a system for providing a plurality of modes and interconnectability between ASICs (application specific integrated circuits) to achieve scaling. A single ASIC includes an input controller section, a memory section, and an output controller section. The ASIC architecture is designed to allow any of the sections to be bypassed. Scalability is provided by interconnecting multiple ASICs, designed on a single board. By combining levels of ASICs, a user can create a system having pluralities of inputs, outputs, and controller ASICs. The pluralities can grow as system requirements grow, often without having to add new memory controller boards. (See, e.g., Abstract and column 1, line 51, through column 2, line 10.) However, unlike the present invention, Gold et al. do not disclose a disk array device that includes storage device control boards having a connection circuit that is connected to a storage device, and switch circuits that are respectively disposed at an input side and an output side of the connection circuit and are switchable

between a connected mode where they are connected to another adjacent storage device control board and an independent mode where they are separated from the other adjacent storage device control board, wherein the switch circuits are switchable between the connected mode and the independent mode by an output signal from a management unit.

U.S. Patent No. 6,425,049 (Yamamoto et al.) discloses a disk array system having a plurality of disk storage apparatuses and a method for changing the configuration of the disk array system. The disk array system has a disk storage group, an array controller, a disk interface connecting unit, and a disk interface connection changing unit. The array configuration may be changed at a user's request by changing the array configuration information. The disk interface connection changing unit sends instruction information on setting up the connection status among the plurality of ports to the disk interface connecting unit to establish the configuration indicated by the array configuration information. The disk interface connecting unit changes the port connection according to the instruction information sent from the disk interface connection changing unit. (See, e.g., Abstract and column 1, line 66, through column 2, line 38.) Thus, Yamamoto et al. includes a single disk interface connecting unit, and Yamamoto et al do not disclose a disk array device that includes storage device control boards having a connection circuit that is connected to a storage device, and switch circuits that are respectively disposed at an input side and an output side of the connection circuit and are switchable between a connected mode where they are connected to another adjacent storage device control board and an

independent mode where they are separated from the other adjacent storage device control board, wherein the switch circuits are switchable between the connected mode and the independent mode by an output signal from a management unit.

U.S. Patent No. 6,813,676 (Henry et al.) discloses a host interface bypass on a fabric-based array controller. The apparatus includes an external electronic device suitable for performing a function, a controller, and a fabric connection. Large storage architectures may use the switched fabric to connect to storage controllers to provide large storage capacities. The disk array control architectures may use a switched fabric to connect modules within the controller. A fabric may be employed in both a storage complex architecture and controller architecture in order to increase performance. (See, e.g., Abstract and column 2, lines 7-19, and column 4, lines 28-39.) However, unlike the present invention, Henry et al. do not disclose a disk array device that includes storage device control boards having a connection circuit that is connected to a storage device, and switch circuits that are respectively disposed at an input side and an output side of the connection circuit and are switchable between a connected mode where they are connected to another adjacent storage device control board and an independent mode where they are separated from the other adjacent storage device control board, wherein the switch circuits are switchable between the connected mode and the independent mode by an output signal from a management unit.

U.S. Patent Publication No. 2001/0054133 (Murotani et al.) discloses a method and a storage unit to control hierarchical management of data migration to maintain balanced performance. A host unit executing two or more applications and disk array controllers are connected by a fabric switch through a fibre channel. The disk array controllers are connected to an external manager which gathers the accessing state through a network. The external manager obtains access data by compiling access data managed by each of the controllers. The external manager communicates with two or more disk array controllers, gathers and manages the access data and the configuration data relating to the physical drives and logical volumes of each disk array controller, and prepares an optimum data migration instruction to equilibrate the access load. (See, e.g., Abstract, paragraph 20, and Figure1.) However, unlike the present invention, Murotani et al. do not disclose a disk array device that includes storage device control boards having a connection circuit that is connected to a storage device, and switch circuits that are respectively disposed at an input side and an output side of the connection circuit and are switchable between a connected mode where they are connected to another adjacent storage device control board and an independent mode where they are separated from the other adjacent storage device control board, wherein the switch circuits are switchable between the connected mode and the independent mode by an output signal from a management unit.

U.S. Patent Publication No. 2002/0023195 (Okada) discloses a disk array apparatus that includes a switch circuit for selectively connecting the disk

apparatus to a disk controller. The switching mechanism comprises: a plurality of array controller connectors connected to a first signal line for a data transfer to and from a plurality of array controllers; a plurality of disk apparatus connectors connected to a second signal line for a data transfer to and from a disk apparatus in which writing and reading of the data is controlled by the array controllers; and a plurality of connection lines for connections between the plurality of array controller connectors and the disk apparatus connectors; a plurality of switch circuits provided on the connection lines for one-to-one connection between the plurality of array controller connectors and the disk apparatus connectors. The switching apparatus further comprises an array controller switching circuit provided in the switch circuits and upon reception a path switching signal from the array controllers, establishing a connection between an array controller corresponding to the path switching signal and the disk apparatus connectors. (See, e.g., Abstract, FIG. 5, and paragraphs 16, 32, 55, and 57.) However, unlike the present invention, Okada does not disclose a disk array device that includes storage device control boards having a connection circuit that is connected to a storage device, and switch circuits that are respectively disposed at an input side and an output side of the connection circuit and are switchable between a connected mode where they are connected to another adjacent storage device control board and an independent mode where they are separated from the other adjacent storage device control board, wherein the switch circuits are switchable between the connected mode and the independent mode by an output signal from a management unit.

U.S. Patent Publication No. 2004/0024951 (Aruga) discloses a computer system incorporating a disk subsystem, a disk array, or a disk drive, which allows high speed transfer by means of arrayed disks connected by a fabric switch. A disk array controller is connected to one disk drive group through a fibre channel fabric switch controller, and to another disk array controller and the disk drive group to separately perform data transfers without interference. When the disk array controller establishes a connection to the disk drive group, the connection between the disk array controller and the disk drive group, the connection between the disk array controller and the disk drive group can operate separately from each other to perform the data transfer at a maximum data transfer rate possible between each disk array controller and respective disk drive unit. (See, e.g., Abstract and paragraphs 14, 15, 38, and Figure1.) However, unlike the present invention, Aruga does not disclose a disk array device that includes storage device control boards having a connection circuit that is connected to a storage device, and switch circuits that are respectively disposed at an input side and an output side of the connection circuit and are switchable between a connected mode where they are connected to another adjacent storage device control board and an independent mode where they are separated from the other adjacent storage device control board, wherein the switch circuits are switchable between the connected mode and the independent mode by an output signal from a management unit.

U.S. Patent Publication No. 2004/0034737 (Fujimoto et al.) discloses a disk array controller is made up of multiple disk array control units for

implementing the data read/write operation and each having channel interface units, disk interface units, cache memory units and shared memory units. The channel interface units and disk interface units and the cache memory units in the multiple disk array control units are connected directly for the portion within each disk array control unit and interconnected for the portion between the cache memory units between the disk array control units by a switch based interconnection which extends across the border of disk array control units, and the channel interface units and disk interface units and the shared memory units are connected directly for the portion within each disk array control unit and interconnected for the portion between shared memory units between the disk array control units by a switch based interconnection which extends across the border of disk array control units. (See, e.g., Abstract and paragraphs 26-28, and 54.) However, unlike the present invention, Fujimoto et al. do not disclose a disk array device that includes storage device control boards having a connection circuit that is connected to a storage device, and switch circuits that are respectively disposed at an input side and an output side of the connection circuit and are switchable between a connected mode where they are connected to another adjacent storage device control board and an independent mode where they are separated from the other adjacent storage device control board, wherein the switch circuits are switchable between the connected mode and the independent mode by an output signal from a management unit.

U.S. Patent Publication No. 2004/0083338 (Moriwaki et al.) discloses a disk array controller that is configured so that it is connected to a plurality of disk

array control units through an inter-connection network consisting of a number of connecting switches determined by the controller. The disk array control unit comprises a plurality of channel interface units connected to a plurality of host computers; a plurality of disk interface units connected to a plurality of magnetic disk drives; a plurality of shared memory units, and a plurality of cache memory units. An inter-connection network consisting of a plurality of connecting switches to connect a plurality of disk array control units is used for the connection between the channel interface units, the shared memory units, and the cache memory units. The other inter-connection network, consisting of a plurality of connecting switches, connects a plurality of disk array control units used for connection between the channel interface units and the cache memory units. These two networks are used to connect a plurality of disk array control units that may be configured independently of each other or united into one. (See, e.g., Abstract and paragraphs 18-20, and 44.) However, unlike the present invention, Moriwaki et al. do not disclose a disk array device that includes storage device control boards having a connection circuit that is connected to a storage device, and switch circuits that are respectively disposed at an input side and an output side of the connection circuit and are switchable between a connected mode where they are connected to another adjacent storage device control board and an independent mode where they are separated from the other adjacent storage device control board, wherein the switch circuits are switchable between the connected mode and the independent mode by an output signal from a management unit.

U.S. Patent Publication No. 2004/0111560 (Takase et al.) discloses a disk array controller capable of connecting storage systems with different architectures to each other in order to manage them as an integrated storage system. A plurality of disk array control units are connected to each other through an inter-unit switch. Each of the disk array control units has an external device connection interface to allow connection with external devices such as host computers, magnetic disks, a shard memory, or a cache memory. The configuration of the disk array controller makes it easier to add more disk array control units. (See, e.g., Abstract and paragraphs 25-26.) However, unlike the present invention, Takase et al. do not disclose a disk array device that includes storage device control boards having a connection circuit that is connected to a storage device, and switch circuits that are respectively disposed at an input side and an output side of the connection circuit and are switchable between a connected mode where they are connected to another adjacent storage device control board and an independent mode where they are separated from the other adjacent storage device control board, wherein the switch circuits are switchable between the connected mode and the independent mode by an output signal from a management unit.

Therefore, since the references fail to disclose a storage device control board to which the storage device is connected, and/or switch circuits that are respectively disposed at an input side and an output side of the connection circuit and are switchable between a connected mode where they are connected to

another adjacent storage device control board and an independent mode where they are separated from the other adjacent storage device control board, and/or the switch circuits are switchable between the connected mode and the independent mode by an output signal from the management unit, and/or in a case where a connected mode instruction/signal is issued from the management unit, the storage devices are together connected to each other and to the same disk adapter, and/or in a case where an independent mode instruction/signal is issued from the management unit, the storage devices are divided into plural storage device groups and the storage device groups are respectively connected to different disk adapters, it is submitted that all of the claims are patentable over the cited references.

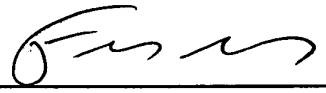
CONCLUSION

Applicant has conducted what it believes to be a reasonable search, but makes no representation that "better" or more relevant prior art does not exist. The Patent Office is urged to conduct its own complete search of the prior art, and to thoroughly examine this application in view of the prior art cited herein and any other prior art that the Patent Office may locate in its own independent search. Further, while Applicant has identified in good faith certain portions of each of the references listed herein in order to provide the requisite detailed discussion of how the claimed subject matter is patentable over the references, the Patent Office should not limit its review to the identified portions but rather, is urged to review and consider the entirety of each reference, and not to rely solely on the identified portions when examining this application.

In view of the foregoing, Applicant requests that this Petition to Make Special be granted and that the application undergo the accelerated examination procedure set forth in MPEP 708.02 VIII.

Respectfully submitted,

MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C.



Frederick D. Bailey
Registration No. 42,282

FDB/sdb
(703) 684-1120

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PETITION FEE
Under 37 CFR 1.17(f), (g) & (h)
TRANSMITTAL
(Fees are subject to annual revision)

Send completed form to: Commissioner for Patents
P.O. Box 1450, Alexandria, VA 22313-1450

Application Number	**10/790,140**
Filing Date	**March 2, 2004**
First Named Inventor	**Hiroshi SUZUKI et al.**
Art Unit	**2182**
Examiner Name	**Not yet assigned**
Attorney Docket Number	**1309.43598X00**

Enclosed is a petition filed under 37 CFR 1.102(d) that requires a processing fee (37 CFR 1.17(f), (g), or (h)). Payment of $ 130.00 is enclosed.

This form should be included with the above-mentioned petition and faxed or mailed to the Office using the appropriate Mail Stop (e.g., Mail Stop Petition), if applicable. For transmittal of processing fees under 37 CFR 1.17(i), see form PTO/SB/17i.

Payment of Fees (small entity amounts are NOT available for the petition (fees)

☒ The Commissioner is hereby authorized to charge the following fees to Deposit Account No. 50-1417:
☐ petition fee under 37 CFR 1.17(f), (g) or (h) ☒ any deficiency of fees and credit of any overpayments
Enclose a duplicative copy of this form for fee processing.

☐ Check in the amount of $ _____ is enclosed.

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Petition Fees under 37 CFR 1.17(f): **Fee $400** **Fee Code 1462**
For petitions filed under:
§ 1.53(e) - to accord a filing date.
§ 1.57(a) - to according a filing date.
§ 1.182 – for decision on a question not specifically provided for.
§ 1.183 – to suspend the rules.
§ 1.378(e) for reconsideration of decision on petition refusing to accept delayed payment of maintenance fee in an expired patent.
§ 1.741(b) – to accord a filing date to an application under §1.740 for extension of a patent term.

Petition Fees under 37 CFR 1.17(g): **Fee $200** **Fee code 1463**
For petitions filed under:
§1.12 - for access to an assignment record.
§1.14 - for access to an application.
§1.47 - for filing by other than all the inventors or a person not the inventor.
§1.59 - for expungement of information.
§1.103(a) - to suspend action in an application.
§1.136(b) - for review of a request for extension of time when the provisions of section 1.136(a) are not available.
§1.295 - for review of refusal to publish a statutory invention registration.
§1.296 - to withdraw a request for publication of a statutory invention registration filed on or after the date the notice of intent to publish issued.
§1.377 – for review of decision refusing to accept and record payment of a maintenance fee filed prior to expiration of a patent.
§1.550(c) – for patent owner requests for extension of time in ex parte reexamination proceedings.
§1.956 – for patent owner requests for extension of time in inter partes reexamination proceedings.
§ 5.12 – for expedited handling of a foreign filing license.
§ 5.15 – for changing the scope of a license.
§ 5.25 – for retroactive license.

Petition Fees under 37 CFR 1.17(h): **Fee $130** **Fee Code 1464**
For petitions filed under:
§1.19(g) – to request documents in a form other than that provided in this part.
§1.84 – for accepting color drawings or photographs.
§1.91 – for entry of a model or exhibit.
§1.102(d) – to make an application special.
§1.138(c) – to expressly abandon an application to avoid publication.
§1.313 – to withdraw an application from issue.
§1.314 – to defer issuance of a patent.

Name (Print/Type)	**Frederick D. Bailey**	*Registration No. (Attorney/Agent)*	**42,282**
Signature		*Date*	April 22, 2005